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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/523,385	02/01/2005	Johannes Otto Voorman	NL 020728	4142

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER

LAMB, CHRISTOPHER RAY

ART UNIT	PAPER NUMBER
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2627

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/523,385

Applicant(s)

VOORMAN ET AL.

Examiner

Christopher R. Lamb

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 January 2007.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 December 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application
- ☐ Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 11th, 2006 has been entered.

Drawings

2. The drawings were received on December 11th, 2006. These drawings are acceptable.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4 and 6-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsuda et al. (US 5,258,968).

Regarding claim 1:

Matsuda discloses:

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An optical disk system comprising at least one photo detector comprising several sub-detectors for detecting at least part of said optical disk (Fig. 9; column 8, lines 1-50),

said at least one photo detector generating detection signals in response to said detection (Fig. 9; column 8, lines 1-50),

the optical disk system further comprising several circuits,

each circuit having an input directly coupled to a respective output of one of said several sub-detectors for receiving said detection signals (apparent from Fig. 9),

said several circuits comprised of at least one amplifier for amplifying detection signals (Fig. 9: 102, 103, 105, 106) and

comprising at least one slicer for slicing amplified detection signals (Fig. 9: 127, 128, 129, 130; column 8, lines 5-20),

the system further comprising at least one delay-difference detector for detecting delay differences in sliced amplified detection signals (Fig. 9: 110),

characterized in that said delay-difference detector is delaylineless (there are no delay lines in Fig. 9) and comprises combinatorial-logic circuits (Fig. 9: 115, 116, 117, 119) and sequential-logic circuits (Fig. 9: 11, 112, 113, 114).

Regarding claim 2:

In Matsuda said delay-difference detector comprises a first pair of sequential-logic circuits for detecting delay differences between rising edges (Fig. 9: 112, 113) and comprises a second pair of sequential-logic circuits for detecting delay differences between falling edges (Fig. 9: 111, 114).

Regarding claim 3:

In Matsuda said delay-difference detector further comprises at least one analog adder/subtractor for adding/subtracting sequential-logic circuit output signals (Fig. 9: 118).

Regarding claim 4:

In Matsuda said delay-difference detector comprises at least one low pass filter coupled to an output of said at least one analog adder/subtractor (Fig. 9: 120).

Regarding claims 6-8:

All elements positively recited have already been identified in the rejection of earlier claims. No further elaboration is necessary.

Regarding claims 9 and 10:

These are method claims corresponding to the earlier apparatus claims and are met when the system operates.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda in view of Ma et al. (US 6,940,799).

Regarding claim 5:

Matsuda discloses an optical disc system as discussed above.

Matsuda does not disclose that "said delay-difference detector comprises at least one low pass filter located between at least one sequential-logic circuit and said at least one analog adder/subtractor."

Note that Matsuda does disclose at least one low pass filter (Fig. 9: 120) as well as the sequential-logic circuit and adder/subtractor. In Matsuda these elements are in a different order: the low-pass filter is after the sequential-logic circuit and the adder/subtractor.

Note also that the sequential-logic circuit of Matsuda is part of differential phase detector (column 8, lines 1-20).

Ma discloses wherein a delay-difference detector comprises at least one low pass filter located between at least one differential phase detector and at least one analog adder/subtractor (Fig. 3b).

It would have been obvious to one of ordinary skill in the art at the time of the invention to include in Matsuda wherein said delay-difference detector comprises at least one low pass filter located between at least one sequential-logic circuit and said at least one analog adder/subtractor.

The motivation is as follows: the two positions of the low pass filter (before or after the adder/subtractor) are equivalents in the art. The two arrangements are used in the same environment, for the same purpose, and achieve the same result.

Furthermore, one of ordinary skill in the art would have expected Applicant's invention to work equally well with either arrangement (Applicant demonstrates this by disclosing both versions).

Response to Arguments

7. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments with regards to the rejections of claims 1-10 as anticipated by Ishibashi or unpatentable over Tateishi in view of Ishibashi were persuasive, and those rejections have been withdrawn. However, a new grounds of rejection has been applied as noted above.

Conclusion

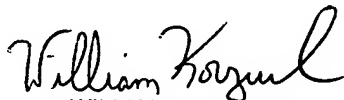
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher R. Lamb whose telephone number is (571) 272-5264. The examiner can normally be reached on 9:00 AM to 6:30 PM Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Korzuch can be reached on (571) 272-7589. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CRL 4/12/07


WILLIAM KORZUCH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600